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Research and Development Technical Report
ECOM - 0039 - 4

MM&T Program for the Establishment of Production Techniques for High Power Bulk Semiconductor Limiters

4TH QUARTERLY REPORT

By

Y. ANAND *R. BILOTTA*

JULY 1977

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MM&T PROGRAM FOR THE ESTABLISHMENT OF PRODUCTION TECHNIQUES FOR HIGH POWER BULK SEMICONDUCTOR LIMITERS

FOURTH QUARTERLY REPORT

23 March 1977 to 22 June 1977

CONTRACT NO. DAAB07-76-C-0039

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FOR

U.S. ARMY ELECTRONICS COMMAND, FORT MONMOUTH, NJ 07703

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X-band bulk limiters of 5 mils in thickness have been fabricated using high resistivity silicon ρ = 26,000 to 32,000 Ω-cm, p-type uncompensated < 111 > orientation from Hughes Industrial Product Division. These bulk limiters exhibit 3 dB bandwidth of 1.05 GHz and power handling capability of 10 to 15 kW at recovery time of 3 to 5 μsec, which is long compared to 2 to 3 μsec for Wacker Chemical material at 10 kW level. During the

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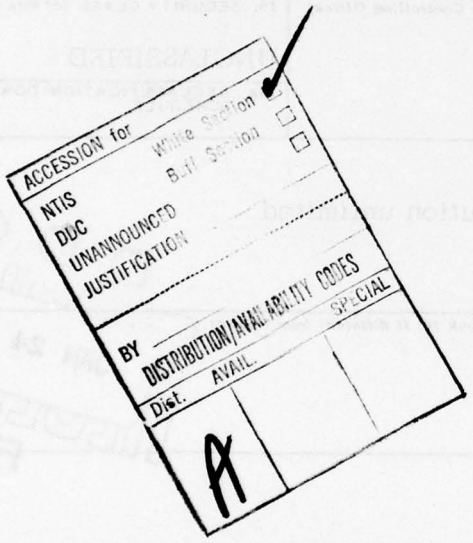
RF testing of bulk limiters at 1 and 3 microsecond pulse widths have shown that pulse energy (peak power x pulse lengths) determines the heating and recovery time.

A new microwave circuit was studied to improve the low-level RF performance of the bulk limiter and diode clean-up limiter.



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ABSTRACT

X-band bulk limiters of 5 mils in thickness have been fabricated using high resistivity silicon ρ = 26,000 to 32,000 Ω-cm, p-type uncompensated < 111 > orientation from Hughes Industrial Product Division. These bulk limiters exhibit 3 dB bandwidth of 1.05 GHz and power handling capability of 10 to 15 kW at recovery time of 3 to 5 μsec which is long compared to 2 to 3 μsec for Wacker Chemical material at 10 kW level. During the fabrication phase, it was further found that Hughes' material etches rougher suggesting higher dislocation density.

RF testing of bulk limiters at 1 and 3 microsecond pulse widths have shown that pulse energy (peak power x pulse lengths) determines the heating and recovery time.

A new microwave circuit was studied to improve the low-level RF performance of the bulk limiter and diode clean-up limiter.

PURPOSE

The objective of this program is to establish a production capability to manufacture High Power Bulk Semiconductor Limiters per U.S. Army Electronics Command Technical Requirements SCS-486.

The specification covers X-band high power bulk semiconductor limiter and low power multistage clean-up limiter. Four fundamental requirements are detailed in the specifications. They are, (1) recovery time, (2) high power capability, (3) insertion loss, and (4) VSWR.

A total of fifteen (15) engineering sample limiters, twenty (20) confirmatory sample limiters and fifty (50) pilot run production limiters will be supplied. A pilot line capable of producing 100 bulk semiconductor limiters per month will be demonstrated. Reports and documentation as required in Sections E, F, G and H of DAAB07-76-Q-0040 and as detailed in Section 3.5 of ECIPPR No. 15, dated December 1976, will be provided.

The program divides into the following four phases, Phase I - Engineering Samples (300 days), Phase II - Confirmatory Sample Production (240 days), Phase III - Pilot Line Production (180 days), and Phase IV - Final Documentation (30 days). The total program duration is 750 days.

During Phase I of this program, a number of factors in fabricating bulk semiconductor limiters are being investigated. These include iris formation, circuit configuration, material characterization and chip mounting. Efforts during Phase I will be directed toward selecting a single limiter design capable of meeting the objectives of SCS-486.

The optimum device design will be chosen at the end of Phase I. In Phases II, III and IV, a single device design will be produced.

The major effort of this program will be realization of a single bulk limiter design which meets all the objectives of SCS-486. Individually, any of the goals described can be currently obtained. Recognizably, it is the development of a single component design which achieves all of the desired performance parameters that is the formidable engineering and manufacturing endeavor.

I. OBJECTIVE

The objective of the current Manufacturing Methods and Technology Engineering program is to establish the producibility of the X-band bulk semiconductor limiter and the X-band bulk semiconductor lower power diode multistage limiter by mass production techniques. Achieving the performance goals of the program represents a formidable engineering task. These goals, from SCS-486, are summarized below.

A. Function Description

The high power, solid state, limiter described herein will operate in the frequency band 9.0 - 9.65 GHz. A multi-stage configuration is acceptable with the first stage incorporating the principle of avalanche breakdown of near-intrinsic silicon to achieve isolation. This device will be mounted in a fixed tuned resonant waveguide cavity designed to provide the necessary avalanche field conditions. The second stage shall be either a bulk effect device or a common semiconductor diode limiter. Both limiter devices will be mounted in a common structure and no external bias or drive will be necessary for its operation. The receiver protector is required to operate in unpressurized conditions.

B. Mechanical Characteristics

The bulk semiconductor limiter structure will have the following performance objectives:

Weight	:	7.0 oz maximum
Input Flange	:	mates with UG-40B/U choke flange
Output Flange	:	mates with UG-135/U cover flange
Mounting Position	:	any
Cooling	:	conduction

C. Electrical Characteristics

The bulk semiconductor limiter will have the following objectives:

Peak RF Input Power	: 30 kW, Du = 0.001
1 μsec Pulses Continuous	: 10 kW, Du = 0.01
Insertion Loss	: 0.7 dB (maximum)
Low Level VSWR	: 1.4:1 (maximum)
Recovery Time	: 0.8 μsec (maximum)
Flat Leakage	: 50 mW (max), for 30 kW, .001 duty cycle, 1 μsec pulse
Spike Leakage	: 750 mW (max), for 30 kW, .001 duty cycle, 1 μsec pulse
External Bias	: none

D. Absolute Rating Objectives

PARAMETER	SYMBOL	MIN	MAX	UNIT
Frequency	F	9.0	9.65	GHz
Peak Power	P	--	30	kW
Average Power	P_a	--	100	W
Ambient Temp.	T_A	-55	+85	^oC
Altitude	--	--	50,000	ft

II. INTRODUCTION

This report covers the period from 23 March 1977 through 22 June 1977. During this period, semiconductor limiter work was concentrated in the areas of semiconductor wafer processing and device fabrication, bulk limiter circuit analysis, and reliability study (life and environmental) of bulk limiters.

Significant improvements in the semiconductor fabrication procedures have been accomplished during the quarter. A batch fabrication scheme was introduced to improve the manufacturability of bulk limiters. The delicate diffusion bonding of the bulk limiter chip to 10 mil gold wire was replaced by ball bonding the gold wire to 3 mil etched gold posts defining the active element area. Difficulties had been encountered in depositing reproducible evaporated metal films, and etching 3 mil gold posts. A metallization problem was overcome by sputtering low energy titanium (10%) - tungsten (90%) alloy and gold films. New high resolution photo mask and photoresist flow techniques were used to obtain reproducible and uniform 3 mil etched gold posts.

Theoretical investigation was carried out to improve the low level RF performance of the bulk and clean-up limiters. The computer model chosen was a simple filter structure consisting of two lumped capacitances and a lumped inductance. In this model, the lumped capacitances were represented by bulk limiters and the lumped inductance physically by an inductive iris. Optimized parameters have been obtained and physical relization of this circuit and experimentation will be conducted during the next quarter.

RF test results showed that it is the pulse energy (peak power x pulse length) which determines the heating and recovery time. Testing of

fifteen samples of 3.5 mil thick, 12 mil diameter Wacker material elements gave 2 - 3 μsec recovery time with either 30 kW - 1 μsec pulses or 10 kW - 3 μsec wide pulses.

The subsequent sections of this report describe in greater detail the work performed and results achieved to date.

III. BULK SEMICONDUCTOR CIRCUIT TUNING ANALYSIS

During this quarter, an attempt was made to improve the low level RF performance of the bulk limiter by studying the computer model.

The model chosen was a simple filter structure consisting of two lumped capacitances and a lumped inductance (see Figure 1). This is a model used very often in broadband coaxial limiter design. In the model, the lumped capacitances represent bulk limiters. The lumped inductance would be physically realized by an inductive iris. It should be mentioned that although a bulk limiter is normally used as a tuned L-C circuit, it can be made capacitive merely by increasing the width of the bulk limiter iris to the full dimension for WR-90 waveguide, 0.900 inches.

The computer program used was a circuit analysis program developed by Microwave Associates. The program allows the designer to solve for the steady-state characteristics of microwave networks composed of transmission lines and networks of capacitors, inductors, and resistors. The network may contain shorted and/or open transmission line stubs in series or shunt with the main transmission line. Circuit branching and modelling of diodes, and transformers is also possible.

The program is relatively simple to use. Being an interactive program, the designer need only supply the computer with information concerning the type of network structure and values for the various impedances, lengths and circuit elements. The convenience of the program is such that it allows the designer to easily change any of these values. Thus, circuit tuning and optimization can be accomplished quite readily.

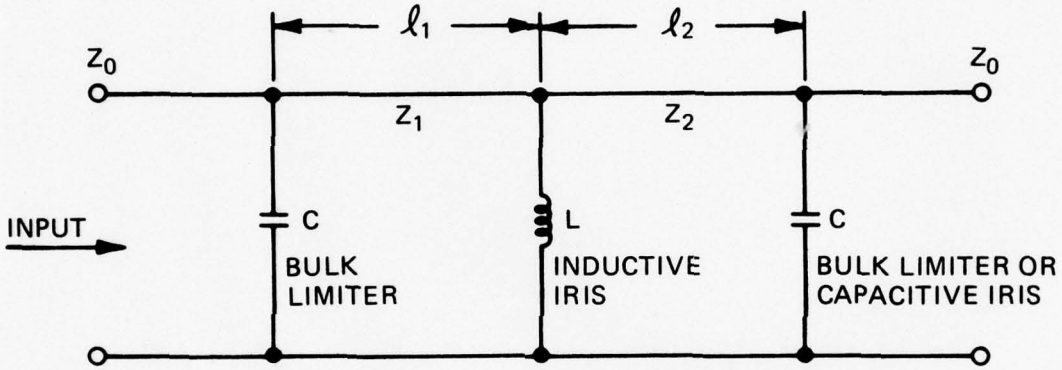

FIGURE 1 CIRCUIT MODEL

Referring to Figure 1, the values for Z_o and C were 471 ohms and 0.25 picofarads, respectively. The value for Z_o was calculated from the equation for waveguide impedance at a point 'd' from one wall. Thus,

$$Z_g = 2 \times \sqrt{\frac{\mu_o}{\epsilon_o}} \times \frac{\lambda_g}{\lambda_o} \times \frac{b}{a} \sin^2 (\pi d/a) \qquad (1)$$

where:

μ_o = permeability of free space

ϵ_o = permittivity of free space

λ_g = guide wavelength

λ_o = free space wavelength

b = waveguide dimension along the narrow wall

a = waveguide dimension along the broad wall

d = point along the broad wall at which the impedance is being calculated

The value for C was a best estimate for the capacitance of the bulk limiter.

The remaining values for Z_1, Z_2, ℓ_1, ℓ_2, and L were varied during the execution of the program in order to optimize the network characteristics.

The results of this effort were very encouraging. The maximum VSWR of the circuit was about 1.2:1 in the frequency range of interest. The final computer printout is shown in Table I. It should be noted at this point that the values for insertion loss were somewhat optimistic as the model did not account for any resistive losses.

The final circuit values are shown in Table II.

FREQUENCY	VSWR	LOSS
8.50	2.942	1.208
8.60	2.246	0.692
8.70	1.760	0.342
8.80	1.426	0.136
8.90	1.201	0.036
9.00	1.054	0.003
9.10	1.037	0.001
9.20	1.086	0.007
9.30	1.091	0.008
9.40	1.050	0.003
9.50	1.032	0.001
9.60	1.166	0.026
9.70	1.374	0.109
9.80	1.682	0.290
9.90	2.132	0.608
10.00	2.779	1.088

TABLE I. Computer Print Out of Circuit Model

PARAMETER	VALUE
C	0.25 picofarads
L	0.18 nanohenries
Z_o	471 ohms
Z_1	515 ohms
Z_2	515 ohms
ℓ_1	0.032 inches
ℓ_2	0.032 inches

TABLE II. Final Circuit Values for the Optimized Model

In summary, the computer model has given us a start toward what we hope will be an improved tuning technique for the entire solid state limiter. Physical realization of this circuit and experimentation will be done during the next work period.

IV. FABRICATION AND RF TEST RESULTS

During the last quarter, ten (10) high resistivity wafers (ρ = 15000 Ω-cm, <111>, p-type uncompensated) from Wacker Chemical and eight (8) wafers (ρ = 26000 Ω-cm, <111>, p-type uncompensated) from Hughes Industrial Products were processed for bulk limiters. These wafers were etched and polished to 5.5 mils in thickness. The phosphorous and boron diffusions were done on both sides of the wafers at 1000°C and 950°C, respectively. The 3/4 mil square checkerboard pattern was used prior to the boron diffusion. Boron nitride source was used as the dopant source during the boron diffusion. Both surfaces of a wafer were then metallized with 500-1000 Å layer of titanium (10%) and tungsten (90%) alloy and 2000-3000 Å layer of gold and then electroplated with pure gold. Both the surfaces were plated to a thickness of 3.0 mils. The active elements area were defined by etching 10 mils in diameter gold posts on the top side of the wafer. The posts were etched to a height of 3 mils using conventional photolithographic and photo-resist flow techniques. The silicon mesa etching process was performed when the elements were still in wafer form. Then the wafer was cut into 40 mil squares and were separated into individual chips. The gold posts of the bulk limiter chips were ball bonded to gold wire (5 mil in diameter). These chips were passivated with silicon nitride and Dow Corning DC-643 Junction Coating. The bulk limiter chips were mounted in gold plated copper X-band irises and were tested for both low and high level RF performance.

A. Summary of RF Results

Bulk limiters were fabricated by varying the wafer thickness, different passivation schemes and by the batch process. These results are summarized in Table III.

Run Number (Wafer Thickness)	Source of Material	Metallization	Insertion Loss dB	Recovery Time τ	Bandwidth GHz	High Power kW	Remarks
BL-15 (3.5 mil)	ρ = 15,000 Ω-cm Wacker	Cr-Au	---	---			Whole run lost through new testing
BL-16A (3.5 mil)	ρ = 15,000 Ω-cm Wacker	Ti-W-Au	0.6	1.5-2.5	0.75	10-15	Good yield, ball bond, good I_V
BL-16B (3.5 mil)	ρ = 15,000 Ω-cm Wacker	Ti-W-Au	1.5	2.0-2.5	0.75	12-15	Fair yield -- high loss, power handling varied
BL-17A (5.5 mil)	ρ = 15,000 Ω-cm Wacker	Ti-W-Au	0.7	2.5-4.5	0.85 -1.15	20 -25	High recovery time 3rd Eng. Samples
BL-17B (5.5 mil)	ρ = 15,000 Ω-cm Wacker	Cr-Au	0.6	2.0-2.5	0.75	10	Not batch process 5.5 mil silicon
BL-17C (5.5 mil)	ρ = 15,000 Ω-cm Wacker	Cr-Au	0.5	2.0-2.5	1.0	10	Batch process 5.5 mil silicon
BL-17D (3.4 mil)	ρ = 15,000 Ω-cm Wacker	Ti-W-Au	0.5	2.0-3.0	1.05	15-20	Power handling varied greatly, long silicon etching
BL-18 (5.5 mil)	ρ = 15,000 Ω-cm Wacker	Ti-W-Au	0.3	2.5-3.5	1.15	5	Resin test to eliminate high loss, poor power handling
BL-19A (5.5 mil)	ρ = 15,000 Ω-cm Wacker	Ti-W-Au	0.9	~10	0.65	15	Repetition rate 330 3 μsec pulse width 12 mil dots

TABLE III. Summary of Various Limiter Runs

Run Number (Wafer Thickness)	Source of Material	Metallization	Insertion Loss dB	Recovery Time τ	Bandwidth GHz	High Power kW	Remarks
BL-19B	ρ = 15,000 Ω-cm Wacker	Ti-W-Au	1.0	6.0-8.0	0.65	10	Repetition rate 330 5.5 mil silicon 3 μsec pulse width 14 mil dots
BL-20-23	ρ = 15,000 Ω-cm Wacker	---	---	---	---		High temperature glass passivation experiments
BL-24A (5.5 mil)	ρ = 26,000 Ω-cm Hughes	Ti-W-Au	0.4	3.5-5.0	1.05	10	Hughes silicon test
BL-24B (5.5 mil)	ρ = 8,000 Ω-cm RRC	Ti-W-Au	0.4	3.5-5.0	1.15	5	RRC silicon test
BL-24C	ρ = 15,000 Ω-cm Walker	Ti-W-Au	0.4	3.5-5.0	1.10	7.5	Walker silicon test

TABLE III. (Cont'd)

B. Recovery Time versus RF Peak Power

Recovery time versus RF peak power of bulk limiters from various runs is given in Table IV and shows that recovery time is dependent upon active area, quality of bonding (heat sink) and the thickness of bulk limiter chips. Higher recovery time was observed for thick (5.5 mils) bulk limiters and large active area diffusion bonded bulk limiters. All these devices were tested with 1 μsec pulse widths and 10^3 pulses per second.

C. Recovery Time versus Pulse Length

RF tests conducted at 1 and 3 microsecond pulse lengths have shown that it is the pulse energy (peak power x pulse length) which determines the heating and recovery time of a bulk limiter. Bulk limiters from Run #19B were tested for recovery time at 1 and 3 μsec pulse lengths at different peak power levels. Results are summarized in Table V and show that bulk limiters gave 6-8 μsec recovery time with either 30 kW - 1 μsec pulses or 10 kW - 3 μsec RF pulses. High recovery time was observed due to 5.5 mil chip thickness and 14 mil active area.

RF tests were repeated with 3.5 mil thick, 12 mil diameter Wacker material, the elements gave 2-3 microsecond recovery time with either 30 kW - 1 μsec pulses or 10 kW - 3 μsec RF pulses.

D. Life and Environmental Test Data

Bulk limiters from Runs BL-16 and BL-17 were subjected to life and environmental tests (Method 1311A - 202E) according to Contract Specifications. Test results are given in Tables VI and VII and show that all units passed the tests without showing any degradation in performance. A bulk limiter BL-17-3 was subjected to 10 kW peak RF power with τ = 1 μsec and 10^3 pulses per second from 200 hours. After the test, the bulk limiter was retested for low-level RF performance and no degradation was observed.

PARAMETERS / PROCESS	BL-12A-5 (μs)	BL-12A-4 (μs)	BL-12A-13 (μs)	BL-12A-15 (μs)	BL-12C, -11 (μs)	BL-12C, -13 (μs)	BL-14A-21 (μs)	BL-16A-21 (μs)	BL-16A-14 (μs)	BL-16A-11 (μs)	BL-16A-13 (μs)	BL-17A-34 (μs)	BL-17A-32 (μs)	BL-17A-I	BL-17A-II	BL-17C$_2$-1	BL-17C$_2$-6	BL-17D-2	BL-17D-11	BL-17D-12	BL-18-5	BL-18-3	BL-19A	BL-19A	BL-19B-1	BL-19B-2
f_o	9.3	9.3	9.4	9.6	9.6	9.6	9.6		9.6	9.6	9.6	9.6	9.6	9.6	9.2	9.6	9.6	9.6	9.6	9.6	9.6	9.6			9.3	9.15
Li (dB)	1.3	1.1	1.0	.9	.5	.6	.7		.8	.7	.5	.6	.5	.6	.5	1.0	.9	.5	.8	.5	.3	.3			.9	1.0
BW (GHz)	.59	.90	.70	.75	.93	.91	.89		.90	1.04	1.05	1.0	.95	1.0	1.25	.70	.75	1.10	.94	1.12	1.25	1.22			.62	.53
Process	Batch	Batch	Batch	Batch	*	*	Batch	Batch	Batch	Batch	Batch	Batch	Batch	Batch	Batch	Batch	Batch	Batch	Batch	Batch					Batch	Batch
Metallization	CrAu	CrAu	CrAu	CrAu	CrAu	CrAu	CrAu	TiWAu	TiWAu	TiWAu	TiWAu	TiWAu	TiWAu	TiWAu	TiWAu	CrAu	CrAu	TiWAu	TiWAu	TiWAu	TiWAu	TiWAu			TiWAu	TiWAu
Bonding	Diff.	Diff.	Diff.	Diff.	Diff.	Diff.	Diff.	Ball	Ball	Ball	Ball	Ball	Ball	Ball	Ball	Ball	Ball	Ball	Ball	Ball	Ball	Ball			Ball	Ball
Chip Thickness (mils)	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	5.5	5.5	5.5	5.5			5	5
POWER (kW)	RECOVERY TIME (τ)																									
1	1.2	1.1	0.9	1.2	0.4	0.5	0.4	0.4	0.8	0.7	0.7	0.7	0.8	0.7	0.8	0.5	0.3	0.5	1.0	1.1	1.7	2.0			2.0	2.3
2	1.3	1.3	1.2	1.4	0.7	.7	0.5	0.5	0.9	0.8	0.9	0.8	1.0	0.9	1.1	0.7	0.5	0.7	1.2	1.4	2.1	2.4			2.3	2.8
5	1.5	1.5	1.4	1.6	1.0	1.0	0.7	0.8	1.2	1.2	1.2	1.0	1.3	1.2	1.8	1.2	0.9	1.1	1.5	1.9	2.7	3.8			3.4	4.0
10	1.7	2.2	1.7	1.8	1.3	1.4	1.0	1.6	1.6	2.3	2.0	1.5	1.7	1.6	4.5	2.0	1.6	1.9	1.8	2.7	--	--			7.2	8.0
15	2.0	3.0	2.0	2.1	2.2	2.0	1.3	--	1.8	2.6	2.7	--	--	2.0	5.7	2.7	2.0	3.2	2.7	3.6	--	--			--	--
20	2.5	3.9	2.4	2.2	3.0	2.8	1.9	--	2.4	3.5	--	--	--	2.4	7.2	--	--	--	3.4	--	--	--			--	--
	NOTE (*): Hughes Wafers																									

TABLE IV. Recovery Time versus RF Peak Power of Various Bulk Limiters

Bulk Limiter Number	f_o (GHz)	Li (dB)	3 dB Bandwidth (GHz)	Pulse Length & Rep. Rate	Repetition Rate	Peak Power	Recovery Time
19B-1	9.3	0.7	0.55	1 μsec	10^3 Hz	30 kW	7 μsec
19B-2	9.3	0.6	0.6	1	10^3	25	6
19B-3	9.3	0.75	0.50	1	10^3	30	7.5
19B-4	9.3	0.8	0.55	1	10^3	30	6
19B-5	9.3	0.65	0.6	1	10^3	25	8
19B-6	9.3	0.7	0.6	3.3 μsec	333 Hz	10 kW	7.5 μsec
19B-7	9.3	0.65	0.55	3.3	333	10	8.0
19B-8	9.3	0.8	0.7	3.3	333	10	6.5
19B-9	9.3	0.7	0.6	3.3	333	10	7.5
19B-10	9.3	0.65	0.5	3.3	333	10	7.0

TABLE V. Recovery Time versus Pulse Length
(Wafer BL-19B -- Wacker material 5.5 mil thick, Ti-W-Au metallization, 14 mil active area etched gold post)

Customer _____
Customer P. O. _____
Part No. _____
Other Dwg. _____
*Methods Per 1311A (202E)

MICROWAVE ASSOCIATES, INC.

Semiconductor Division

#	LOT DATE CODE

M/A Type _____
Class _____
M/A SO No. _____

	PROGRAM REQUIREMENTS								Estimated		Actual		REMARKS	Test Oper.
	Examination/Test	Method No.	Test Conditions		QTY	REJECTS	NET	Test Limits	Start Date	Comp. Date	Start Date	Comp. Date		
	Temperature Cycling	1027	-55°C to +100°C		4			one cycle	5/25	5/25			non-operating	
	Vibration	(204C)	Method A 10 G; 10-500-10Hz					12X/plane X, Y & Z	5/26	5/27			sweep frequency range in 15 minutes	
	Shock	(213B)	Method G 50 G; t = 11 msec					3 shocks/plane $X_1, X_2, Y_1, Y_2, Z_1, Z_2$	6/07	6/07			sawtooth waveform	
	Humidity	(202)	80-90% Humidity -10°C to +65°C					1 cycle	7/07	7/07				

TABLE VI. Life & Environmental Test Schedule/Summary

ENVIRONMENTAL TEST

Product No.	Original Readings			Shock & Vibration			Temperature			Humidity		
	F_o	LI @ F_o	BW	F_o	LI @ F_o	BW	F_o	LI @ F_o	BW	F_o	LI @ F_o	BW
BL-16A-1	9.6	0.6dB	0.78GHz	9.6	0.7dB	0.77GHz	9.6	0.7dB	0.77GHz	9.6	0.7dB	0.77GHz
BL-16A-3	9.6	0.6dB	0.75GHz	9.6	0.6dB	0.76GHz	9.6	0.6dB	0.76GHz	9.6	0.6dB	0.77GHz
BL-17-1	9.05	0.6dB	0.97GHz	9.03	0.6dB	0.93GHz	9.05	0.6dB	0.93GHz	9.03	0.6dB	0.92GHz
BL-17-2	9.2	0.5dB	1.25GHz	9.17	0.6dB	1.22GHz	9.15	0.6dB	1.22GHz	9.15	0.5dB	1.20GHz

LIFE TEST

	Original Readings			200 Hours @ 10 kW			
BL-17-3	9.6	0.5dB	1.05GHz	9.6	0.5	1.05GHz	

TABLE VII. Life & Environmental Test

V. PROBLEM AREAS

A. Recovery Time

The recovery times obtained with both single and dual slot bulk limiters have been in the order of 1.5 to 2 microseconds. This may be reduced by geometry changes being incorporated in the batch fabrication work currently underway.

VI. DELIVERIES

During the quarter, we delivered Third Engineering Sample diodes (Item 0001AA) to the U.S. Army Electronics Command. These included five (5) X-band semiconductor bulk limiters and a clean up limiter. The electrical test data of these diodes is given in Table VIII.

PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS - 3940XM	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 1	OF 3

SPECIFICATION SCS-486 LOT SIZE 5 SALES ORDER NO.

PARAMETERS	fo	Li	3dB Band-width			Li	VSWR	Band-width							
TEST CONDITIONS		@fo				9.0GHz to 9.65	9.0GHz to 9.65								
MIN. LIMITS	--	--	--			--	--	--							
MAX. LIMITS	(GHz)	--	(GHz)			.8dB	1.4:1	(GHz)							
	Bulk	Limiter	Alone												
S/N 17ALE-2	9.300	.4	1.20												
S/N 17ALE-3	9.300	.5	1.22												
S/N 17ALE-4	9.310	.4	1.22												
S/N 16A-13	9.300	.5	1.15												
S/N 17A-34	9.310	.4	1.030												
S/N															
S/N		Bulk	Limiters in Package with Clean-up Limiter												
S/N 17ALE-2						1.4	1.47	.640	@ 1.47:1						
S/N 17ALE-3						1.1	1.44	.650	@ 1.44:1						
S/N 17ALE-4						1.3	1.45	.650	@ 1.45:1						
S/N 16A-13						1.4	1.56	.650	@ 1.56:1						
S/N 17A-34						1.6	1.70	.630	@ 1.70:1						
						TABLE VIII.									

TESTED BY: DATE: Q. C. APPROVED BY: DATE:

FORM 707-C

PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS - 3940XM	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 2	OF 3

SPECIFICATION SCS-486 LOT SIZE 5 SALES ORDER NO.

PARAMETERS	P_F	P_S	R_T		P_F	P_S	R_T		P_F	P_S	R_T				
TEST CONDITIONS	Du = .001 T_P = 1.0 µs Frequency = 9.0GHz PIN = 5.5 kW				Du = .001 T_P = 1.0 µs Frequency = 9.3GHz PIN = 5.5 kW				Du = .001 T_P = 1.0 µs Frequency = 9.6GHz PIN = 5.5 kW						
MIN. LIMITS	-	-	-		-	-	-		-	-	-				
MAX. LIMITS	(w)	(w)	(µs)		(w)	(w)	(µs)		(w)	(w)	(µs)				
	Bulks Limiters Alone														
S/N 17ALE-2	100	200	2.0		40	200	2.6		50	200	3.0				
S/N 17ALE-3	50	160	2.0		40	200	2.6		50	200	3.0				
S/N 17ALE-4	40	200	1.5		40	200	1.8		45	200	2.0				
S/N 16A-13	40	160	1.4		40	200	1.6		40	200	1.8				
S/N 17A-34	31	100	1.2		31	100	1.2		40	100	1.4				
S/N															
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TABLE VIII. (Cont'd)

TESTED BY: DATE: Q. C. APPROVED BY: DATE:

FORM 707-C

PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS - 39040XM	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 3	OF 3

SPECIFICATION SCS-486 LOT SIZE 5 SALES ORDER NO.

PARAMETERS	P_F	P_S	R_T	P_b		P_F	P_S	R_T	R_b		P_F	P_S	R_T	P_b	
TEST CONDITIONS	Du = .001 tp = 1.0 µsec Frequency = 9.0GHz PIN = 5.5 kW					Du = .001 tp = 1.0 µsec Frequency = 9.3 GHz PIN = 5.5 kW					Du = .001 tp = 1.0 µsec Frequency = 9.65 GHZ PIN = 5.5 kW				
MIN. LIMITS	-	-	-	-		-	-	-	-		-	-	-	-	
MAX. LIMITS	50mw	.75w	.8µs	(mw)		50mw	.75w	.8µs	(mw)		.50mw	.75mw	.8µs	(mw)	
	Bulk Limiters in Package with Clean-up Limiter														
S/N 17ALE-2	<10	.250	2.6	20		<10	.250	2.7	18		<10	.250	2.6	15	
S/N 17ALE-3	<10	.250	2.6	18		<10	.250	2.7	16		<10	.250	3.0	<10	
S/N 17ALE-4	<10	.250	1.8	15		<10	.250	2.0	18		<10	.250	2.0	18	
S/N 16A-13	<10	.250	1.6	16		<10	.250	1.6	20		<10	.310	1.8	<10	
S/N 17A-34	<10	.250	1.2	16		<10	.250	1.2	18		<10	.250	1.4	16	
S/N															
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TABLE VIII. (Cont'd)

TESTED BY: DATE: Q. C. APPROVED BY: DATE:

FORM 101 C

VII. CONCLUSIONS

X-band bulk limiters have been fabricated using high resistivity silicon with ρ = 15,000 to 20,000 Ω-cm, p-type, uncompensated from Wacker Chemical Company and ρ = 26,000 to 32,000 Ω-cm, p-type, uncompensated from Hughes Industrial Products Division. Bulk limiters from Hughes' wafer exhibited 3 dB bandwidth of 1.05 GHz and power handling capability of 10 to 15 kW at recovery time of 3-5 microseconds which is long compared to 2 to 3 μsec for the Wacker Chemical material at 10 kW. Third Engineering Samples were fabricated using Wacker high resistivity material and were shipped on schedule.

The Life and Environmental Study is being conducted on various bulk limiters. Various fabrication processes are being optimized to achieve both bandwidth and RF goals of the contract.

VIII. PROGRAM FOR THE NEXT QUARTER

During the next quarter, we will fabricate devices using low cost stamped irises. Batch process and ball bonding techniques will be optimized to improve the yield of good quality bulk limiters. Experimental evaluation of the computer model circuit will also be carried out.

IX. IDENTIFICATION OF PERSONNEL

During this quarter, the following technical personnel contributed to this program.

Title	Manhours
Project Manager	150
Silicon Materials Manager	15
Senior Processing Engineer	40
Processing Engineer	30
Limiter Engineer	60
Engineering Assistant (Fabrication)	150
Engineering Assistant (Test)	250

Electronic Command

Technical Requirements

SCS-486

28 March 1975

High Power Bulk Semiconductor Limiter

1. SCOPE: This specification describes a passive, solid state, receiver protector using a bulk semiconductor limiter in combination with a semiconductor diode limiter. Limiter operation will provide isolation from x-Band pulses up to 30 kw over a variety of test conditions.

2. APPLICABLE DOCUMENTS

2.1 Documents. - The following documents, of issue in effect on the date of invitation for bids, form a part of this specification to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-E-1	General Specification for Electron Tube
MIL-P-11268	Parts, Materials, and Processes Used in Electronic Equipment

STANDARDS

MILITARY

MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-202	Test Methods for Electronic and Electrical Components Parts

MIL-STD-1311A Microwave Oscillator Test Methods

(Copies of specifications, standards and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer. Both the title and number of symbol should be stipulated when requesting copies.)

FSC 5961

REQUIREMENTS:

3.1 Function Description. - The high power, solid state, limiter specified herein will operate in the frequency band 9.0 - 9.65 GHZ. A multi-stage configuration is acceptable with the first stage incorporating the principle of avalanche breakdown of near-intrinsic silicon to achieve isolation. This device will be mounted in a fixed tuned resonant waveguide cavity designed to provide the necessary avalanche field conditions. The second stage shall be either a bulk effect device or a semiconductor diode limiter. Both limiter devices will be mounted in a common structure and no external bias or drive will be necessary for its operation. The receiver protector is required to operate in unpressurized conditions.

3.2 Mechanical Characteristics. - The bulk semiconductor limiter structure will conform to the following requirements:

(a)	Weight	20 oz max
(b)	Input flange	mates with UG-40B/U choke flange
(c)	Output flange	mates with UG-135/U cover flange
(d)	Mounting position	any
(e)	Cooling	conduction

3.2.1 Physical Dimensions. - The bulk semiconductor limiter shall conform to Figure 1.

3.2.2 Construction. - Parts and materials will be in accordance with MIL-P-11268.

3.3 Electrical characteristics. - The bulk semiconductor limiter will conform to the following requirements:

(a)	Peak Rf Input power, 1μsec pulses continuous	:	30 kw, Du = .001 10 kw, Du = .01
(b)	Insertion Loss	:	0.7dB (max)
(c)	Low Level VSWR	:	1.4:1 (max)
(d)	Recovery Time	:	0.8μsec (max)
(e)	Flat Leakage	:	50 mw (max), for 30 kw, .001 duty cycle, 1μsec pulse
(f)	Spike Leakage	:	750 mw (max), for 30 kw, .001 duty cycle, 1 μsec pulse
(g)	external bias	:	none

3.4 Absolute Ratings

Parameter	Symbol	Min	Max	Unit
Frequency	F	9.0	9.65	GHZ
Peak Power	P		30	kw
Average Power	Pa		100	w
Ambient Temp.	T_A	-55	+85	°C
Altitude	—		50,000	ft

3.5 Marking. - Each bulk semiconductor limiter shall be marked with the following information:

(a) Manufacturer's model number

(b) Manufacturer's serial number, individually for each limiter.

(c) rf input port.

(d) rf output port.

4. QUALITY ASSURANCE PROVISIONS

4.1 Inspection.

4.1.1 Responsibility for inspection. - The contractor is responsible for the performance of all inspection requirements as specified herein. The contractor may utilize his own facilities or any commercial laboratory acceptable to the government. The government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements. Inspection records of the examinations and tests shall be kept complete and available to the government.

4.1.2 Test equipment & inspection facilities. - Test equipment and inspection facilities shall be of sufficient accuracy, quality, and quantity to permit performance of the required inspection. The supplier shall establish calibration of inspection equipment to the satisfaction of the government.

4.2 Classification of inspection. - The examination and testing of limiters shall be classified as follows:

a. First article inspection (see 4.3).

b. Quality conformance inspection (see 4.4.).

4.3 First article inspection. - First article inspection shall be performed by the supplier, after award of contract and prior to production at a location acceptable to the government. It shall be performed on sample units which have been produced with equipment and procedures which will be used in production. This inspection shall consist of QCI-1, QCI-2 and QCI-3 inspection in accordance with 4.4.1, 4.4.2 and 4.4.3.

4.3.1 Sample. - Twenty (20) limiters shall be submitted for first article inspection.

4.4 Quality Conformance Inspection.

4.4.1 Quality conformance inspection - Part 1 (QCI-1). - Every limiter shall be tested in all positions of the Quality Conformance Inspection - Part 1 (QCI-1). No failures shall be permitted.

4.4.2 Quality conformance inspection - Part 2 (QCI-2). - The Quality Conformance Inspection - Part 2 (QCI-2) shall be performed in accordance with MIL-STD-105, Inspection Level S1 with an AQL of 6.5%. In the event of lot rejection, tightened inspection procedures shall be invoked. Normal inspection shall be resumed when two (2) consecutive lots have conformed with QCI-2 tests. If the lot size is less than 50 limiters, the sample size shall be one (1) with an acceptance number of zero (0). For purposes of inspection, the lot size shall be one (1) month's production.

4.4.3 Quality conformance inspection - Part 3 (QCI-3). - Three limiters shall undergo continuous life testing for a min. of 2500 hrs. No failures shall be permitted.

4.5 Detailed listings of quality conformance inspection tests. - Quality conformance inspection tests shall be conducted in accordance with Table I (QCI-1), Table II (QCI-2), and Table III (QCI-3).

Test Conditions

Parameter / Unit	T_A °C	Fo GHZ	Po Watts	μ sec	P_{RR} Pulses/sec	Du	Watts
TC 1	25±3	9.0, 9.375, 9.65±.01	30,000 ± 500	1.0±0.1	1000±25	.001	30
TC 2	25±3	9.0 - 9.65 ± .01	0.001	CW	—	—	—
TC 3	25±3	9.0, 9.375, 9.65±.01	—	1.0±0.1	1000±25	.001	—
TC 4	25±3	9.0, 9.375, 9.65±.01	10,000 ± 250	1.0±0.1	10,000 ±150	.01	100
TC 5	25±3	9.375±.01	30,000 ± 500	1.±0.1	1000 ±25	.001	30
TC 6	—	—	0	—	—	—	—
TC 7	25±3	—	0	—	—	—	—

	Mil Standard	Application Method	Test Condition	Symbol	Limits Lower	Limits Upper	Units	Notes
Maximum Leakage (flat)	1311A	4452A	TC 1	P_f		50	mw	1,3
Maximum Leakage (spike)	1311A	4452A	TC 1	P_s		750	mw	2,3
Insertion Loss	1311A	4416	TC 2	Li		0.7	db	3,4
Low Level VSWR	1311A	4473	TC 2	σ		1.4:1	—	3,4,5
Recovery Time	1311A	4471B (Method B)	TC 1	τ		0.8	μ sec	3,8
Firing Power	1311A	4496	TC 3	P_{FR}		150	mw	3,6,8

Quality Conformance Inspection - Part 1 (QC 1-1)

Table II

	Mil Standard	Application Method	Test Condition	Symbol	Limits Lower	Limits Upper	Unit	No.
Maximum Leakage (flat)	1311A	4452A	TC 1	P_f	—	100	W	1,7
Maximum Leakage (spike)	1311A	4452A	TC 1	P_s	—	400	W	2,7
Maximum Leakage (flat)	1311A	4452A	TC 4	P_f	—	50	mw	1,3
Maximum Leakage (spike)	1311A	4452A	TC 4	P_s	—	750	mw	2,3
Recovery Characteristic(phase)	—	—	TC 5	ΔR_p	—	0.5	degree	3,8,9
Recovery Characteristic (amplitude)	—	—	TC 5	ΔR_a	—	0.1	db	3,8,9
Temperature Cycling(non-oper.)	1131A	1027	TC 6	ΔL_i Δf_3 $\Delta \gamma$	—	0.2 100 0.2	db mw μ sec	10
Vibration	202E	204C Method A	TC 7	ΔL_i Δf_3 $\Delta \gamma$	—	0.2 100 0.2	db mw μ sec	10
Shock	202E	213B Method G	TC 7	ΔL_i Δf_3 $\Delta \gamma$	—	0.2 100 0.2	db mw μ sec	10
Humitity	1311A	1011	TC 6	ΔL_i Δf_3 $\Delta \gamma$	—	0 0 0	db mw μ sec	10

	Mil Standard	Application Method	Test Condition	Symbol	Limits Lower	Limits Upper	Unit	Notes
Life Test	1311A	4551A	TC 5	t	2500		hours	11
Life Test End-Point (1)	1311A	4452A	TC 1	P_s		1.0	watt	2,3
Life Test End-Point (2)	1311A	4416	TC 2	L_i		0.9	db	3,4
Life Test End-Point (3)	1311A	4471B	TC 1	γ		1.0	μ sec	3
Life Test End-Point (4)	1311A	4452A	TC 1	P_f		75	mw	1,3
Life Test End-Point (5)	1311A	4496	—	P_{FR}		170	mw	3,6

Quality Conformance Inspection - Part 2 (QC111-3)

)TES:

)e maximum flat leakage shall not exceed the specified limits for test frequencies 9 000, 9.375, .9.650GHZ. The incident Rf pulse will have a risetime 50 nanoseconds maximum. Test configuration reference figure 4452 - 1b. The peak power measurement will be accomplished by calibrating the deflection of a sampling oscilloscope as described in section 3.2 paragraphs 3.2.1 and 3.2.2 of Mil-Std-1311A.

The maximum spike leakage shall not exceed the specified limits for test frequencies 9.000, 9.375, 9.650 GHZ. Oscilloscope calibration technique as described in section 3.2 paragraphs 3.2.1 and 3.2.2 of Mil-Std-1311A is applicable. Amplitude variation shall be recorded by observing the distribution of spike amplitudes for 1 minute time through open shutter of scope camera.

Quality conformance test to be made using multi-stage limiter. For example using the high power bulk stage followed by the limiter diode.

A swept frequency may be used.

Match Termination used in this test circuit shall have a VSWR of 1.05 or less.

The firming power shall be defined as a db increase of limiter insertion loss mpared to the "cold" insertion loss.

Quality conformance test to be made using bulk semiconductor stage only.

For this specification the following abbreviations and symbols in addition to MIL-E-1 abbreviations and symbols shall apply; τ = time (recovery), ΔR_p = variation of phase on recovery (total deviation at a fired time), ΔR_a = variation of amplitude on recovery (total deviation at a fixed time), P_{FR} = firing power.

The maximum variation in phase and amplitude as measured by dynamic phase and amplitude test facility shall not vary more than the specified limits over a 1 minute integration time period. Measurement to be made at a point 5μsec from the cessation of 1μsec input pulse.

). Measurement of parameters cited will follow the procedures outlined in QCI -1.

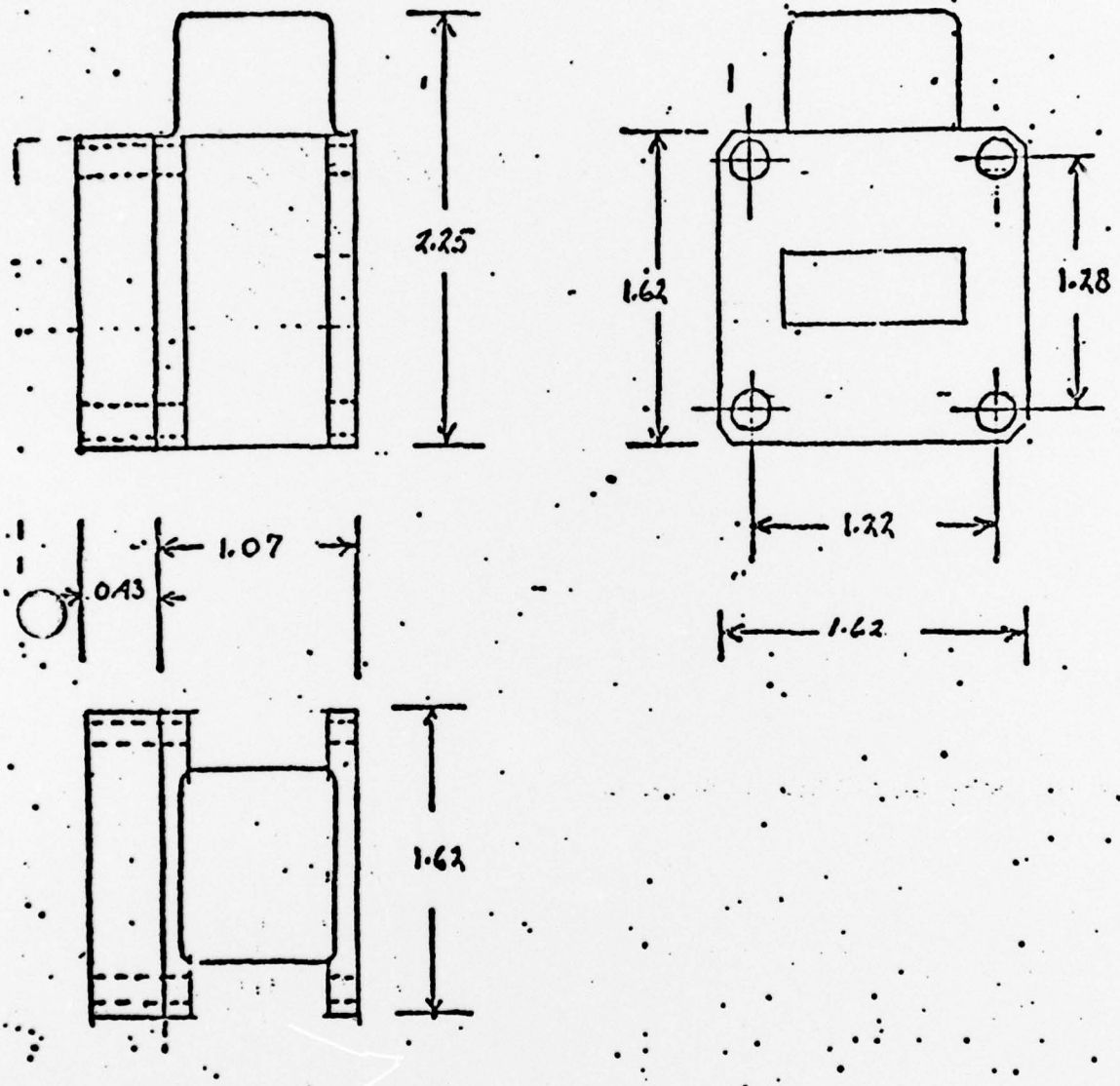
1. The bulk semiconductor limiter shall operate over the entire duration of the life test. The spike leakage (P_s) will be periodically monitored. Life test will be interrupted each 720 ± 20 hours intervals to permit testing of end of life test end points.

5. PREPARATION FOR DELIVERY

5.1 Packaging, Packing and Marking. - Packaging, packing and package arking shall be specified in the contract.

FIGURE 1

LINE DRAWING



Notes:

a) all dimensions in inches

b) all tolerances ± 0.01 unless otherwise specified

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